THE MACHINE CSIRAC

by

T.M. Cherry and F. Hirst
Department of Applied Mathematics
University of Melbourne, Victoria

1. SKETCH OF THE COMMAND FACILITIES

CSIRAC has a word-length of 20 bits, which for the coding of commands is partitioned as follows:

Standard weighting 2^0 2^{-1} . . . . 2^{-19}

p_{20} p_{19} . . . p_{11}	p_{10} . . . p_6	p_5 . . . p_1
address (cell-number)	source	destination

This is a 2-address system. Most commands call for the transfer (symbolized $\rightarrow$) of the word in a 'source' register (or of some part of this word) to another 'destination' register: either a straight transfer, or admission to the destination register through an adding, subtracting or multiplying gate. There are 18 registers (called $A, C, D_0, D_1, \ldots D_{15}$) into which, as destinations, a word can be added or subtracted (or simply transferred); and from these 18, as sources, can be read out either the word or its sign digit or its right-shift.

The address digits $p_{20} \cdots p_{11}$ specify which cell is to be called in a command involving as source or destination either the high speed (mercury line) store or one of the four magnetic disc tracks; each of these 5 stores has capacity for 1024 words. These digits are used also to specify which of the 16 D registers is involved in a command having (D), s(D), or r(D) as source or D, + D or − D as destination.

The machine is thus effectively a multi-accumulator machine.

In written programmes a functional symbolism - as opposed to a purely numerical code or the barbarous typewriter code - is used, whereby the meaning of the commands springs to the eye; the translation from the written code to pulse patterns is made automatically, of course, via the keyboard punch and the tape.

Examples:

$69 : (M) \xrightarrow{+} A$	add the word in store cell 69 into register A and hold the sum.
$4 : s(C) \rightarrow D_4$	transfer the sign digit of the word in C to register D_4
$4 : s(D_4) \xrightarrow{+} D_4$	replace the sign digit of the word in D_4 by 0
$64 : r(C) \rightarrow M$	transfer the word in C, right-shifted one place, to store cell 64.

Selection of commands, normally from consecutive high-speed store cells, is controlled by the sequence register S (which holds half-words $p_{20} \cdots p_{11}$ only), and breaks in the normal sequential selection are made by explicit operations on the sequence register. For this purpose there are three operations having S as a destination, viz. transfer to S, addition into S, and 'count into S'; for this last, a sign digit that has been read out from any source (in p_{20} position necessarily) is converted into a p_{11} digit before adding it into S.

Examples:

$s\,(D_0) \xrightarrow{c} S$	if D_0 is positive, proceed sequentially; if negative, skip one command.
$(S) \rightarrow D_{15}$	to store the number in S, prior to entering a closed routine.

The interpreter register K, whose normal use is to decode command-words, has two supplementary uses; (1) as a source of constants, in the 'upper-half' position p ... p , by a command such as m: $(K) \rightarrow A$; (2) for variable modification of a command (the 'B line facility') by a sequence such as

1. $(D_4) \xrightarrow{+} K$ 2. 0 ; $(M) \rightarrow A$	if D_4 holds the word m: 0, 0, command 2 becomes m; $(M) \rightarrow A$. Normally these will be part of a loop which will include a command for progressive alteration of the word in D4.

For the specially important constants p_{20}, p_{11}, p_1 there are special sources.

Amongst the special commands may be mentioned absolute and conditional stops, zero-test for register A, and multiple left-shift for the double length product-register A,B.

2. COMMENTS

CSIRAC was designed about 1948 by T. Pearcey and is of similar vintage to EDSAC I. It was built in the Radiophysics Laboratory in Sydney, and came into service in 1952-3. Its maximum speed is about 400 commands per second.

Its advantages are, notably, ease of programming and ease of finding programme errors; for the latter, a programme can be run 'single-shot', and there are monitor-screens on which can be conveniently seen the contents of all registers and store cells. Its disadvantages are its short word-length, slow speed, and the lack of operations (other than multiplication and left-shift) on a double-length accumulator.

Because of its many accumulators there is a saving of commands as compared with a single-address machine, but this is partly offset because a conditional change of control nearly always takes 2 commands as against EDSAC's 1 command. There is however an overall saving of about 10 per cent.

Routines have of course been developed for the commonly required operations, including function-blocks for double length and floating arithmetic.

The machine has been extensively used for calculations relating to scientific research and "public service".

3. LIST OF SOURCES AND DESTINATIONS

Code	No.	Source	Destn.	Code	No.	Source	Destn.
0	M	(high speed store)	M	3	N_2	(hand-set input)	O_p (output, punched)
1	I	(tape input)	spare				
2	N_1	(hand-set input)	O_t (output, printed)	4	A	(main accumulator)	A
				5	s(A)	(sign digit)	+A

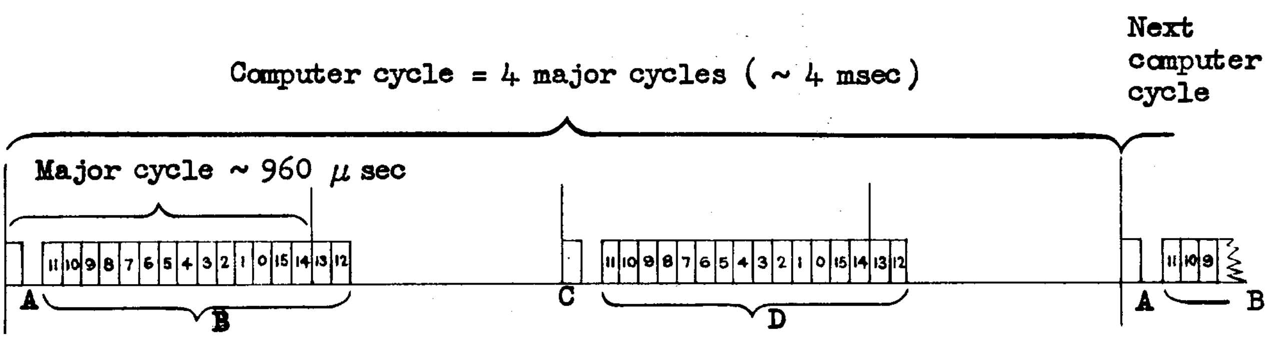
Code No.		Source	Destn.
6	$\frac{1}{2}$(A)		−A
7	2(A)	(left shift)	.A(conjunction)
8	p_1(A)	(bottom digit)	vA(disjunction)
9	$\underline{c}$(A)	(read and clear)	≠A(nonidentity)
10	z(A)	(zero-test)	P(speaker)
11	B	(lower half of product register)	B
12	R	(rounding digit)	XB(multiply)
13	r(B)	(B right shifted)	L(left shift A,B)
14	C	(multiplier)	C
15	s(C)		+C
16	r(C)		−C
17	D		D

Code No.		Source	Destn.
18	s(D)		+D
19	r(D)		−D
20	Z	(zero constant)	spare
21	H_l	{for half word-length shifts}	H_l
22	H_u		H_u
23	S	(sequence reg.)	S
24	p_{11}		+S
25	p_1		cS
26	K	(interpreter)	+K
27	M_a	(magnetic disc tracks)	M_a
28	M_b		M_b
29	M_c		M_c
30	M_d		M_d
31	p_{20}		T(stop)

4. PHYSICAL DETAILS

4.1 Computer cycle.

The digit pulses of the machine are nominally 50 volts in amplitude, about $\frac{3}{4}$ μsec. in width, and spaced 3 μsec. A minor cycle or word length of 20 digits is thus 60 μ sec, and 16 word-lengths constitute a major cycle. With normal operation, 4 major cycles are required for the performance of a command. The time to perform one command is designated a computer cycle which is illustrated in Fig. 1.



COMPUTER CYCLE

Fig. 1

Referring to the legend of Fig. 1, the computer cycle is as follows:-

(A) During this minor cycle, the sequence register digits representing the cell number of the command to be performed are gated to the memory cell selector.

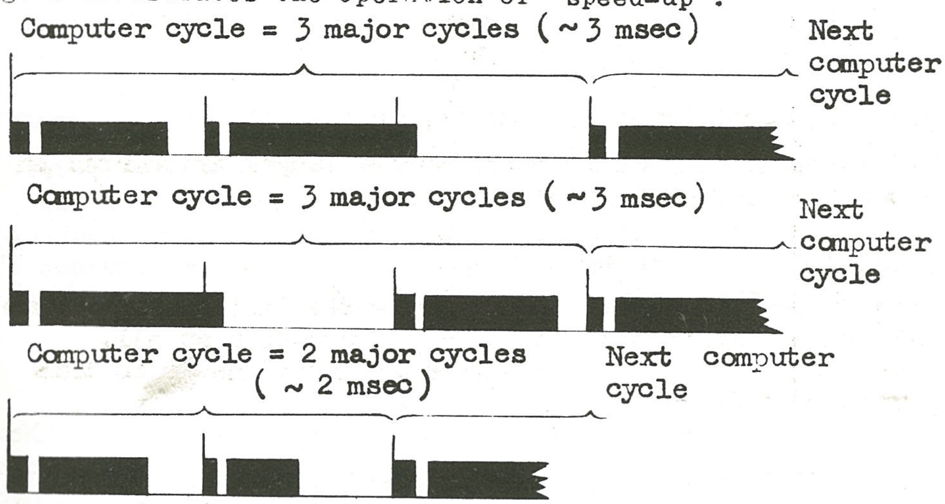
(B) The appropriate command is transferred from memory to the interpreter during one of the 16 minor cycles of B, this minor cycle being selected by the action of A. After B has been completed, the source and destination gates are activated.

(C) The address of the command in the interpreter is read out and sets up the memory controls appropriately.

(D) The command is performed during one of the 16 minor cycles selected by the address.

In the address part of a command the $p_{11} - p_{14}$ digits designate the time position of the command in a memory loop (viz. 0-15), whilst the $p_{15} - p_{20}$ digits refer to the particular loop involved.

There is provision for the machine to perform commands on "speed-up". With this mode of operation the period of the computer cycle may be reduced by either one or two major cycles. If the cell number of a command in the memory does not involve the time positions 14, 13, 12, economy of one major is effected. Again if the address of the command does not involve these time positions the same economy is achieved. When both of the above conditions apply simultaneously, economy of two major cycles is obtained. Fig. 2 illustrates the operation of "speed-up".



EFFECT OF SPEED-UP

Fig. 2

It is to be noted that "speed-up" is always inhibited for multiplication which requires a fixed period of about 4 m/sec. for its completion. All other commands require a computer cycle of about 2, 3, or 4 milliseconds.

4.2 Mercury memory.

In the mercury memory separate delay lines are employed allowing defective components to be replaced easily. Each delay line is about 55 ins. long and represents a delay of 960 μsec. thereby accommodating 16 words. The carrier frequency is 10 Mc/sec. and the quartz crystals are backed with hard lead blocks to give a band pass of 5 Mc/sec. whilst reducing the first echo to a suitable level.

Originally the pulse spacing was set at 3 μsec to achieve satisfactory operation of the flip-flops using 6SN7 valves. Because of the adequate band pass, the shape of the pulses emerging from a delay line is maintained sufficiently to allow them to be interspaced by a separate digit train without interference. This expedient increases the capacity of a mercury line twofold, and a 1024 cell memory is achieved using only 32 delay lines.

The mercury store is housed in a hot-box held at ambient summer temperature (36° C), a special frequency control delay line being used to maintain the main computer clock in synchronism with the memory. A separate hot-box contains the short delay lines used for the dynamic registers.

4.3 Completed instruction store (C.I.S. unit)

A 16 word delay line is used to store the sequence numbers, sources and destinations of the last 16 completed commands. This information can be displayed on a monitor tube and is extremely valuable for diagnostic purposes.

4.4 Magnetic memory

This is in the form of a rotating disc (7 ins. radius) and is of the asynchronous type. Both sides are employed and a storage of 4096 words is provided. The speed of rotation is 3000 revs/min giving an average access time of about 10 milliseconds.

DISCUSSION

Dr. J.H. Wilkinson, National Physics Laboratories.

Do you find yourself frequently doing double length arithmetic on this machine due to its 20 bit numbers?

Dr. T.M. Cherry (In Reply)

During our experience with the machine over the last year, we have not had to use double length arithmetic very frequently at all. However, Pearcey may be able to give a more explicit answer to this with his experience at Sydney.

Dr. T. Pearcey, C.S.I.R.O.

At Sydney we found we did not often have to go to double length arithmetic. It was our standard practice to normally work in single length arithmetic and when not to go to floating arithmetic.

Mr. H. Orde, National Cash Register.

I see you have three logical instructions in your order code. Were they put in because the engineers thought they might be useful or because Pearcey thought they would be useful in programming?

Dr. T.M. Cherry (In Reply)

This is a very difficult question to answer, but I think that we can say that we have found effective uses for all of them.